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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,112	06/24/2003	Richard K. Williams	ATI002US	3705

27906 7590 09/29/2005

PATENT LAW OFFICES OF DAVID MILLERS
6560 ASHFIELD COURT
SAN JOSE, CA 95120

EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,112	WILLIAMS ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1:704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-17,26 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-9* is/are allowed.

6)☒ Claim(s) *2-6,10-17,26 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/1/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed on July 1, 2005.

Allowable Subject Matter

The indicated allowability of claims 2, 5, and 9 is withdrawn in view of the newly discovered reference(s) to Williams et al. (US 6,049,108) and Kocon (US 6, 198,127 B1). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 2, 3, 6, and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Kocon (US 6,198, 127 B1).

In re claim 2, Kocon shows (fig. 2) a semiconductor device comprising: a substrate (216) of a first conductivity type (N), the substrate including a plurality of trenches (202a) (col. 1, lines 50-63), a first region (207) of a second conductivity type (P) adjacent to at least one of the trenches, the first region extending to a first depth in the substrate and including a channel region adjacent to the trenches; a second region

(212) of the second conductivity type (P) wherein the second region is in electrical contact with the first region (by contact with the source metal 215); and the second region extends to a second depth that is deeper than the first depth and shallower than the trenches. A gate structure (203) is formed in the plurality of trenches in the substrate, wherein in each of the trenches the gate structure comprises a conductive gate (205) surrounded by an insulating material (204, 206) that has a first thickness at a sidewall (202a) of the trench and a second thickness at a bottom (202b) of the trench, the second thickness being greater than the first thickness, and wherein the conductive gate extends to a depth that is deeper than the first depth and shallower than the second depth. A third region (211) of the first conductivity type (N) is atop the first region, wherein a voltage on the conductive gate controls a current flow from the third region through the first region to an underlying portion of the substrate.

In re claim 3, Kocon shows (fig. 2) that the substrate comprises a first semiconductor layer (201a) atop a semiconductor substrate that is more heavily doped (N+) than the first semiconductor layer (N), wherein the trenches extend into the first semiconductor layer.

In re claim 6, Kocon discloses (col. 1, lines 11-33 and fig. 2) that the voltage on the conductive gate (205) controls a current flow from the third region (214) through the first region (207) and through the first semiconductor layer (208) to the semiconductor substrate (216).

In re claim 10, Kocon shows (fig. 2) that the first region and the third region are in a first mesa between a first pair of trenches (a trench of the plurality would be formed to

the left of the first trench) and the second region (212) is between a second pair of trenches (a trench of the plurality would also be formed to the right of the first trench).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kocon (US 6,198,127 B1) in view of Williams et al. (US 6,049,108). .

In re claim 5, Kocon shows (fig. 2) a semiconductor device comprising: a substrate (216) of a first conductivity type (N), the substrate comprising a first semiconductor layer (201) atop the semiconductor substrate, wherein the semiconductor substrate is more heavily doped than the first semiconductor layer, and a plurality of trenches (202a) (col. 1, lines 50-63) in the substrate that extend into the first semiconductor layer. A gate structure (203) is formed in the plurality of trenches in the substrate, wherein in each of the trenches the gate structure comprises a conductive gate (205) surrounded by an insulating material (204, 206) that has a first thickness at a sidewall (202a) of the trench and a second thickness at a bottom (202b) of the trench, the second thickness being greater than the first thickness. The device also comprises a first region (207) of a second conductivity type (P) adjacent to at least one of the trenches, the first region extending to a first depth in the substrate and

including a channel region adjacent to the trenches, wherein the first region forms a first junction with the second semiconductor layer and a second region (212) of the second conductivity type (P) wherein the second region is in electrical contact with the first region (by contact with the source metal 215), the second region extending to a second depth that is deeper than the first depth and shallower than the trenches. The second region also forms a second junction with the first semiconductor layer. A third region (211) of the first conductivity type (N) is atop the first region, wherein a voltage on the conductive gate controls a current flow from the third region through the first region to an underlying portion of the substrate. Kocon shows all of the elements of the claims except the substrate further comprising a second semiconductor layer atop the first semiconductor layer, wherein the second semiconductor layer is more lightly doped than the first semiconductor layer. Williams et al. shows (fig. 4) a semiconductor device comprising a second semiconductor layer (Nepi2) formed on a first semiconductor layer (Nepi1), wherein the second semiconductor layer is more lightly doped than the first semiconductor layer (col. 7, lines 21-27). The device also includes a second region (38) that forms a second junction with the first semiconductor layer (14). With this configuration, the breakdown voltage of the subsequent diodes formed between the trenches is optimized (col. 8, lines 12-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the substrate of Kocon by adding a second semiconductor layer being more lightly doped than the first semiconductor layer as taught by Williams to optimize the breakdown voltage of the diodes between the trenches.

In re claim 27, Williams shows (fig. 4) that the second junction (between 28 and N-epi layer 14) is laterally separated from the trenches.

Claim 4, 11, 14, 17, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kocon (US 6,198,127 B1) as applied to claim 2 above, and further in view of Williams et al. (US 6,049,108).

In re claim 4, Kocon shows all of the elements of the claims except the substrate further comprising a second semiconductor layer atop the first semiconductor layer, wherein the second semiconductor layer is more lightly doped than the first semiconductor layer. Williams et al. shows (fig. 4) a semiconductor device comprising a second semiconductor layer (Nepi2) formed on a first semiconductor layer (Nepi1), wherein the second semiconductor layer is more lightly doped than the first semiconductor layer (col. 7, lines 21-27). With this configuration, the breakdown voltage of the subsequent diodes formed between the trenches is optimized (col. 8, lines 12-20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the substrate of Kocon by adding a second semiconductor layer being more lightly doped than the first semiconductor layer as taught by Williams to optimize the breakdown voltage of the diodes between the trenches.

In re claim 11, Williams shows (fig. 4) that the device further comprising a fourth region (P+ region not labeled between trench 31B and 31C) of the second conductivity

type, wherein the fourth region is at a surface of the substrate and extends across an entire separation between the second pair of trenches.

In re claim 14, Williams shows (fig. 4) that a second region (38) extends to a first plurality of adjacent mesas that are between pairs of the trenches (31B and 31C) and is absent from a second plurality of adjacent mesas that are between pairs of the trenches (31C and 31D).

In re claim 17, Williams shows (fig. 4) that the second region (38) has a concentration of dopants (P+ doped) of the second conductivity type that is higher than that of the first region (33 being P doped).

In re claim 26, Williams shows (fig. 4) that the first region (33) forms a junction at the first depth; and the second region (38) forms a junction that is at the second depth and laterally separated from the trenches.

Claims 12 and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Kocon (US 6,198,127 B1) as applied to claim 2 above, and further in view of Hshieh et al. (US 5,689,128).

In re claim 12, Kocon does not show the complete semiconductor device having the fourth and fifth regions between two adjacent trenches. Hshieh et al. shows (fig. 2) a mesa between a first and a second of the trenches (24) comprising: the third region (20) at a surface of the substrate and adjacent to the first trench; a fourth region (20) of the first conductivity type at the surface of the substrate and adjacent to the second trench (rightmost trench 24); a fifth region (18 in the middle) of the second conductivity type

between the third and fourth regions at the surface of the substrate; the first region (36 middle) underlying the third and fourth regions. The second region (36) underlies the third region (20) and is separated from first and second trenches (24) to reduce the occurrence of a parasitic JFET (col. 4, lines 7-13). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the second region of Kocon by forming that second region separate from the first and second trenches as taught by Hshieh to eliminate parasitic JFET action.

In re claim 13, Hshieh shows (fig. 2) an electrical contact (30) to the third, fourth, and fifth regions.

Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kocon (US 6,198, 127 B1) as applied to claim 2 above, and further in view of Calafut et al. (US 6,396,102).

In re claims 15 and 16, Kocon shows all of the elements of the claims but does not specifically show the device further comprising a gate bus that is electrically connected to the gate structure in the trenches, wherein the gate bus overlies a portion of the substrate that includes at least part of the first region or the second region. Calafut et al. shows (fig. 4F) a trenched MOSFET having a bus surface structures 46a, 46b, 46c) over the trenches and connected to the gates within the trench. These surface structures provide a voltage to the gates within the trenches. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the trenched gates of Kocon by connecting a gate bus structure to the trenched

gates and over the regions of the substrate as taught by Calafut to provide a voltage to the gates in the trenches.

Allowable Subject Matter

Claims 7-9 are allowed.

The following is an examiner's statement of reasons for allowance: In re claim 7, the prior art references, alone or in combination, do not show a semiconductor device comprising a substrate having a layer in which trenches reside, the layer having a graded dopant profiles such that a concentration of dopants of the first conductivity type, increases with depth in the layer. Furthermore, in re claim 9, the prior art does not show a first region of a second conductivity type adjacent to at least one of a plurality of trenches, the first region extending to a first depth in the substrate, a semiconductor device comprising a second region of the second conductivity type, wherein the second region comprises a series of implantations at varying depths, is in electrical contact with a first region, and extends to a second depth that is deeper than the first depth and shallower than the trenches formed in the substrate.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments with respect to claims 2-6 and 10-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Darwish et al. (US 5,674,766) and Hshieh et al. (US 5,558,313) also show semiconductor devices having second semiconductor layers being more lightly doped than a first semiconductor layer and the substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW

September 20, 2005

Tom Thomas

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SUPERVISORY PATENT EXAMINER